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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,956	10/31/2005	Wolfgang Clemens	411000-137	8177

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EXAMINER	
ARORA, AJAY	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/541,956	CLEMENS ET AL.	
	Examiner	Art Unit	
	Ajay K. Arora	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/06 & 2/5/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 9-11, 14-18 and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi (US 2001/0046081) hereinafter Hayashi

Regarding claim 1, Hayashi (refer to Figures 1A-1F, 2A-2E, 3C, 3D and 4A-4F) teaches a circuit board arrangement for an organic electronic device, comprising:

a circuit board (page 6, para 0117 and page 8, para 0148) having a surface on which a plurality (page 8, para 0148, 3rd sentence) of electrically interconnected electrical devices are disposed;

at least one of the electrical devices comprises an active organic (page 8, para 0147) electronic component (with source electrode 33, as shown in Figure 4C) electrically integrated on the surface with others of the interconnected devices to form at least a portion of an electrical circuit; the organic electronic component having at least one electrode layer (31, see Figure 4c);

the at least one electrode layer of the integrated active organic electronic component forming a conductive track layer (16b of Figures 3C or 3D) on the surface for an inorganic (page 8, para 0151, first sentence) semiconductor electrical component (page 8, para 148, 1st sentence and para 149).

Regarding claim 2, Hayashi teaches a circuit board arrangement for an electronic device comprising:

a circuit board (page 6, para 0117 and page 8, para 0148) defining a surface; and

at least one active organic (page 8, para 0147) electrical component (with source electrode 33, as shown in Figure 4C) and at least one passive organic electrical component (page 8, para 0149, 2nd last sentence) integrated to form at least a portion of an electrical circuit on the surface.

Regarding claim 3, Hayashi teaches that the at least one active electrical component is an organic transistor (page 8, para 0147 or para 151, 1st sentence), and/or the passive organic component is an electrically conducting connection (page 8, para 0149, 2nd last sentence).

Regarding claim 4, Hayashi teaches that the device includes a power supply (page 8, para 0144, 1st sentence) integrated with the electrical circuit on the surface (page 8, para 0145, 1st sentence).

Regarding claim 5, Hayashi teaches that the substrate wherein an input element (page 6, para 0112 and para 0113) and/or an output element (page 6, para 0110)) is integrated on the substrate.

Regarding claim 6, Hayashi teaches that the electrically conductive lines or conducting contacts are on the surface using structured conductive layers, and/or conductive adhesives and which may form electrodes for the electrical components (page 8, para 0147, 1st and 2nd sentence).

Regarding claim 7, Hayashi teaches an visualization element and/or a display (Col. 4, lines 52 and 55) is integrated on the substrate.

Regarding claim 9, Hayashi teaches that a driver circuit associated with the display is electrically integrated on the surface with the circuit (page 8, para 0146).

Regarding claim 10, Hayashi teaches that the driver circuit comprises at least one organic field-effect transistor (page 8, para 0151, 1st sentence).

Regarding claim 14, Hayashi teaches that a driver electronics is included and comprises at least one organic field-effect transistor (page 8, para 0151, 1st sentence).

Regarding claims 11, 15-18, 20 and 21, the claims merely recite use language. The device of Hayashi, which is a display device, is capable of being used at least as a price marker.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 12, 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi in view of Antoniadis (US 6,366,017), hereinafter Antoniadis.

Regarding claim 8, Hayashi teaches that the display comprises electrochromic material (page 6, para 0125) or liquid crystalline elements (page 6, para 0124, 2nd sentence), However, Hayashi does not teach that the display comprises organic light-emitting diodes. Antoniadis US (6,366,017) teaches the use the use of organic light-emitting diodes in displays (Col. 1, lines 10-15). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Hayashi so that the display comprises electrochromic material, liquid crystalline elements and/or organic light-emitting diodes. The ordinary artisan would have been motivated to modify Hayashi for

at least the purpose of optimizing display design taking advantage of the good resolution resulting from liquid crystal elements, the ability to use non-transparent substrates with organic light-emitting diode, and the reduced power consumption advantage of electrochromic materials.

Regarding claim 12, Hayashi teaches that a driver circuit associated with the display is electrically integrated on the surface with the display (page 8, para 0146).

Regarding claim 13, Hayashi teaches that a driver electronics is included and comprises at least one organic field-effect transistor coupled to the circuit (page 8, para 0151, 1st sentence).

Regarding claim 19, the claims merely recite use language. The device of Hayashi, which is a display device, is capable of being used at least as a price marker.

Response to Arguments

Applicant's arguments filed 01/26/2007 have been fully considered but they are not persuasive.

On page 8, applicant argues that "Circuit boards do not comprise laminated layers as disclosed, but rather a single insulating substrate on which interconnected printed circuits and devices are mounted". This argument is not persuasive. Circuit boards

may be single layer or multi-layer; and multi-layer circuit boards may comprise multiple laminated layers. The definition of a circuit boards provided by the applicant as "an insulated board on which interconnected circuits and components such as microchips are mounted or etched" also does state that a circuit board cannot be multi-layer. Multilayer circuit boards are described in various documents, including US 6407344 titled "Multilayer Circuit Board" to Horiuchi et. Al.

On page 10, applicant argues that "No active organic electronic component is shown on the layer 16d" and appears to conclude that an active organic component is not disclosed. This argument is not persuasive. As referenced in the rejection of claim 1, (page 8, para 0147) specifically discloses forming a transistor, wherein "the organic conductive layer 31 forms a gate electrode" and "an organic semiconductor layer layer 35" are formed. This etablishes that an active organic electronic component is disclosed.

On page 12, applicant argues that "This structure requires the organic component to have a conductive track layer on the surface for an inorganic semiconductor electrical component. This structure is missing in Hayashi". This argument is not persuasive. As referenced in the rejection of claim 1, a conductive track layer (16b of Figures 3C or 3D) on the surface for an inorganic (page 8, para 0151, first sentence) semiconductor electrical component (page 8, para 148, 1st sentence and para 149) is disclosed. Further, referring to (page 8, para 149), the 2nd sentence describes the conductive track

layer (16b) and the interconnection between layers; and (page 8, para 0151, 1st sentence) discloses at least one inorganic semiconductor electrical component (i.e. a silicon integrated circuit chip) that is interconnected.

On page 12, applicant argues that "No inorganic semiconductor component, however, is disclosed in Figure 3C or this paragraph or anywhere else in the reference". This argument is not persuasive. As mentioned earlier, (page 8, para 0151, 1st sentence) discloses at least one inorganic semiconductor electrical component (i.e. a silicon integrated circuit chip).

All other arguments on page 12 or later to the extent claimed have already been addressed above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sara W Crane

Sara Crane
Primary Examiner